Quad Matched 741-Type Operational Amplifiers

OP11

FEATURES

Guaranteed V_{OS}: 500 µV maximum
Guaranteed matched CMRR: 94 dB minimum
Guaranteed matched V_{OS}: 750 µV maximum
LM148/LM348 direct replacement
Low noise
Silicon-nitride passivation
Internal frequency compensation
Low crossover distortion
Continuous short-circuit protection
Low input bias current

PIN CONFIGURATION

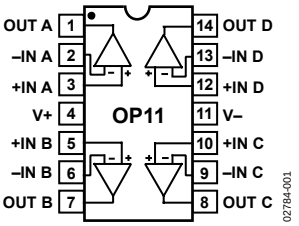

Figure 1. 14-Lead PDIP (N-14)
(P Suffix)

GENERAL DESCRIPTION

The OP11 provides four matched 741-type operational amplifiers in a single 14-lead PDIP. The OP11 is pin compatible with the LM148, LM348, RM4156, RM4158, and HA4741 amplifiers. The amplifier is matched for common-mode rejection ratio and offset voltage, which is very important in designing instrumentation amplifiers. In addition, the amplifier is designed to have equal positive-going and negative-going slew rates, which is an important consideration for good audio system performance.

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The OP11 is ideal for use in designs requiring minimum space and cost while maintaining performance.

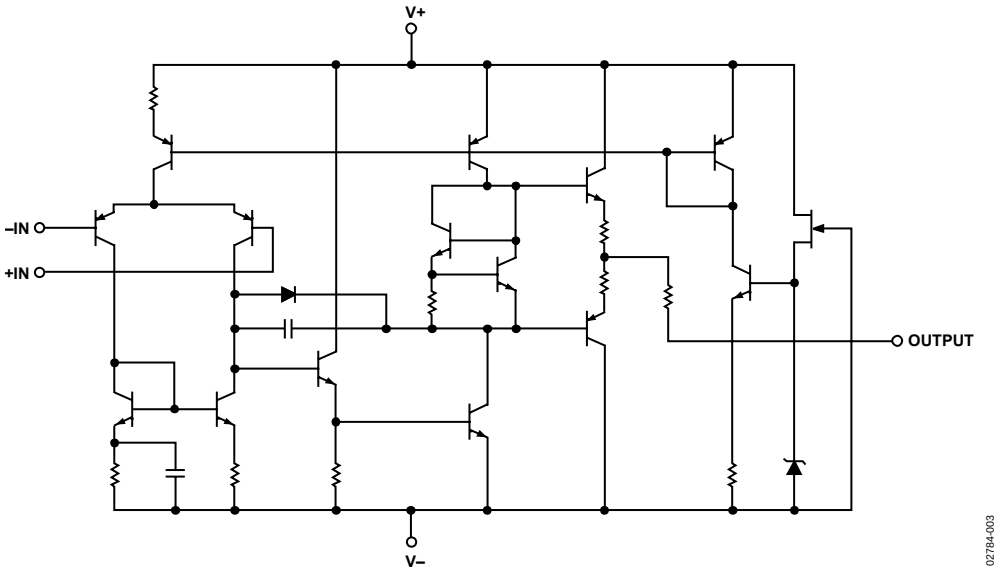

Figure 2. Simplified Schematic

Rev. B
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One Technology Way, P.O. Box 9106, Norwood, MA 02062-9106, U.S.A.
Tel: 781.329.4700 **www.analog.com**
Fax: 781.461.3113 **©2007 Analog Devices, Inc. All rights reserved.**

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REVISION HISTORY

6/07—Rev. A to Rev. B

Updated Format ..... Universal
Deleted 14-Lead Hermetic DIP/CERDIP ..... Universal
Changes to Table 1 3
Deleted Table 3; Renumbered Sequentially 3
Changes to Table 2, Layout, Table 3, and Table 4 4
Changes to Table 5 and Table 6 5
Changes to Figure 17 8
Updated Outline Dimensions 9
Changes to Ordering Guide 9

4/02—Rev. 0 to Rev. A

Change OP-09/OP-11 to OP11 ..... Global
Edits to Pin Connections 1
Edits to Figure 1 1
Edits to Absolute Maximum Ratings 2
Edits to Ordering Guide 2
Edits to Spec Tables 2-4
Deletion of Dice Characteristics 5
Deletion of Wafer Test Limits Table 5
Deletion of Typical Electrical Characteristics Table 5

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SPECIFICATIONS

ELECTRICAL CHARACTERISTICS

V_S = ±15 V, T_A = 25°C, unless otherwise noted.

Table 1.

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Input Offset Voltage	V_{OS}	$R_S \leq 10$ kΩ		0.3	0.5	mV
Input Offset Current	I_{OS}			5.5	20	nA
Input Bias Current	I_B			180	300	nA
Input Resistance Differential Mode[1]	R_{IN}		0.17	0.29		MΩ
Input Voltage Range	IVR		±12	±13		V
Common-Mode Rejection Ratio	CMRR	V_{CM} = ±12 V, $R_S \leq 10$ kΩ	100	120		dB
Power Supply Rejection Ratio	PSRR	V_S = ±5 V to ±15 V, $R_S \leq 10$ kΩ		4	32	μV/V
Output Voltage Swing	V_O	R_L = 2 kΩ	±11	±13		V
Large Signal Voltage Gain	A_{VO}	$R_L \leq 2$ kΩ, V_O = ±10 V	100	650		V/mV
Power Consumption[2]	P_d	V_O = 0 V		105	180	mW
Input Noise Voltage	e_n p-p	0.1 Hz to 10 Hz		0.7		μV p-p
Input Noise Voltage Density	e_n	f_O = 10 Hz		18		nV/√Hz
		f_O = 100 Hz		14		nV/√Hz
		f_O = 1 kHz		12		nV/√Hz
Input Noise Current	I_n p-p	0.1 Hz to 10 Hz		17		pA p-p
Input Noise Current Density	I_n	f_O = 10 Hz		1.8		pA/√Hz
		f_O = 100 Hz		1.5		pA/√Hz
		f_O = 1 kHz		1.2		pA/√Hz
Channel Separation	CS		100	130		dB
Slew Rate[3]	SR		0.7	1.0		V/μs
Large Signal Bandwidth[3]		V_O = 20 V p-p	11	16		kHz
Closed-Loop Bandwidth[4]	BW	A_{VCL} = 1	2.4	3.0		MHz
Rise Time[3]	t_f	A_V = 1, V_{IN} = 50 mV		110	145	ns
Overshoot[3]	OS			15	25	%

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[1] Guaranteed by input bias current.
[2] Total dissipation for all four amplifiers in package.
[3] Sample tested.
[4] Guaranteed by rise time.

V_S = ±15 V, 0°C ≤ T_A ≤ 70°C, unless otherwise noted.

Table 2.

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Input Offset Voltage	V_{OS}	R_S ≤ 10 kΩ		0.4	0.8	mV
Average Input Offset Voltage Drift[1]	TCV_{OS}	R_S ≤ 10 kΩ		2.0	10	µV/°C
Input Offset Current	I_{OS}			14	30	nA
Average Input Offset Current Drift[1]	TCI_{OS}			0.1	0.3	nA/°C
Input Bias Current	I_B			200	350	nA
Input Voltage Range	IVR		±12	±13		V
Common-Mode Rejection Ratio	CMRR	V_{CM} = ±12 V, R_S ≤ 10 kΩ	100	120		dB
Power Supply Rejection Ratio	PSRR	V_S = ±5 V to ±15 V, R_S ≤ 10 kΩ		4	32	µV/V
Large Signal Voltage Gain	A_{VO}	R_L ≥ 2 kΩ, V_O = ±10 V	50	250		V/mV
Output Voltage Swing	V_O	R_L ≥ 2 kΩ	±11	±13		V
Power Consumption[2]	P_d	V_O = 0 V		115	200	mW

[1] Guaranteed but not tested.
[2] Total dissipation for all four amplifiers in package.

MATCHING CHARACTERISTICS

V_S = ±15 V, T_A = 25°C, R_S ≤ 100 Ω, unless otherwise noted.

Table 3.

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Input Offset Voltage Match	ΔV_{OS}			0.5	0.75	mV
Common-Mode Rejection	ΔCMRR	V_{CM} = ±12 V		1	20	µV/V
Ratio Match		V_{CM} = ±12 V	94	120		dB

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V_S = ±15 V, 0°C ≤ T_A ≤ 70°C, R_S ≤ 100 Ω, unless otherwise noted.

Table 4.

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Input Offset Voltage Match	ΔV_{OS}			0.6	1.0	mV
Common-Mode Rejection	ΔCMRR	V_{CM} = ±12 V		3.2	20	µV/V
Ratio Match		V_{CM} = ±12 V	94	110		dB

ABSOLUTE MAXIMUM RATINGS

Table 5.

Parameter	Rating
Supply Voltage (V_S)	±22 V
Differential Input Voltage	±30 V
Input Voltage	Supply Voltage
Output Short-Circuit Duration	Continuous (One Amp Only)
Storage Temperature Range	−65°C to +125°C
Lead Temperature (Soldering, 60 sec)	300°C
Operating Temperature Range	0°C to 70°C

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Table 6. Thermal Resistance

Package Type	θ_{JA}[1]	θ_{JC}	Unit
14-Lead PDIP (N-14)	83	39	°C/W

[1] θ_{JA} is specified for worst-case conditions, that is, θ_{JA} is specified for device in socket for PDIP.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

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TYPICAL PERFORMANCE CHARACTERISTICS

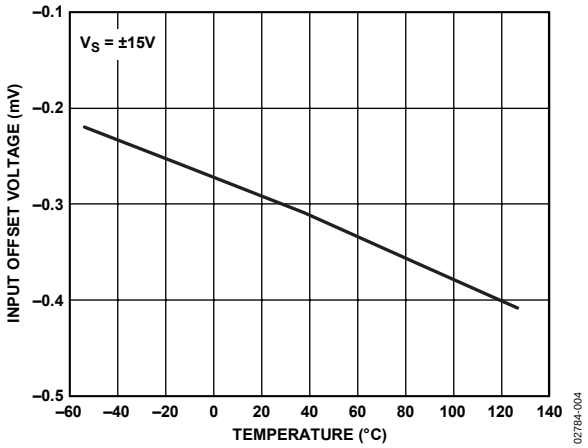

Figure 3. Input Offset Voltage vs. Temperature

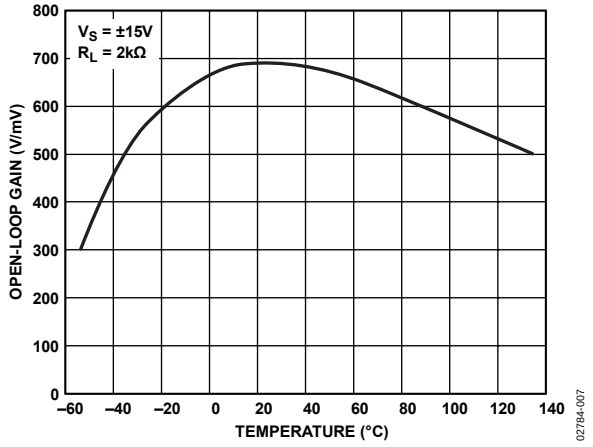

Figure 6. Open-Loop Gain vs. Temperature

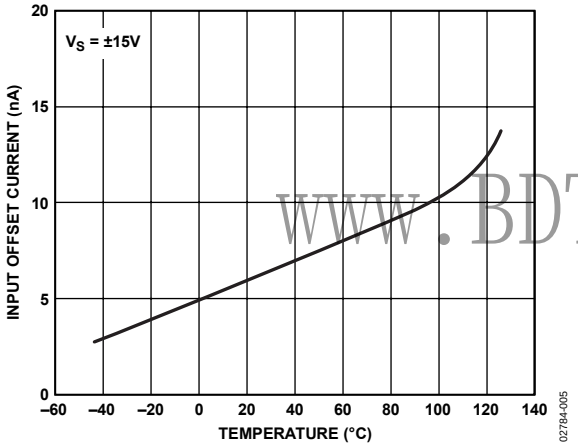

Figure 4. Input Offset Current vs. Temperature

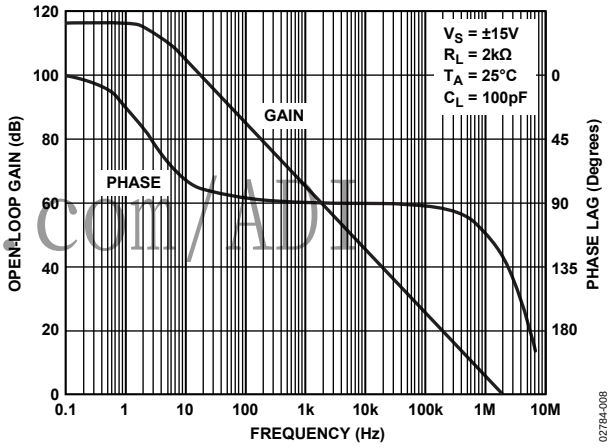

Figure 7. Open-Loop Gain and Phase vs. Frequency

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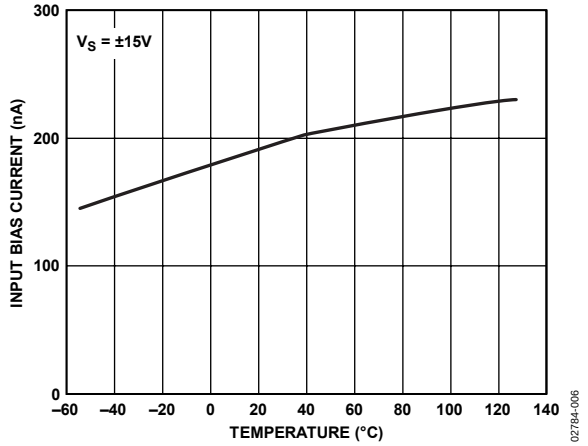

Figure 5. Input Bias Current vs. Temperature

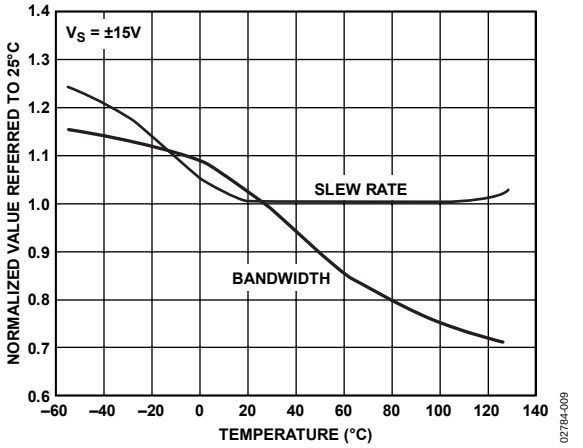

Figure 8. Normalized Slew Rate and Bandwidth vs. Temperature

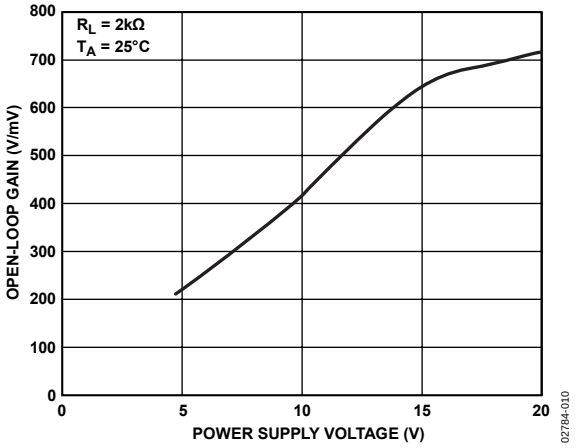

Figure 9. Open-Loop Gain vs. Power Supply Voltage

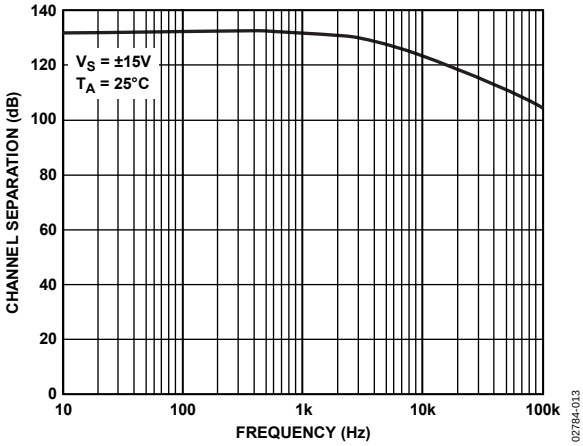

Figure 12. Channel Separation vs. Frequency

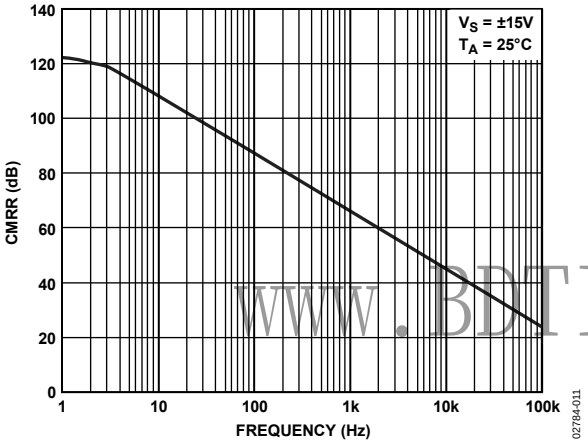

Figure 10. CMRR vs. Frequency

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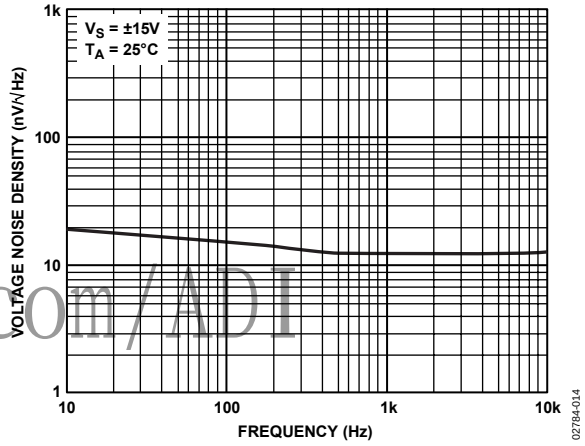

Figure 13. Voltage Noise Density vs. Frequency

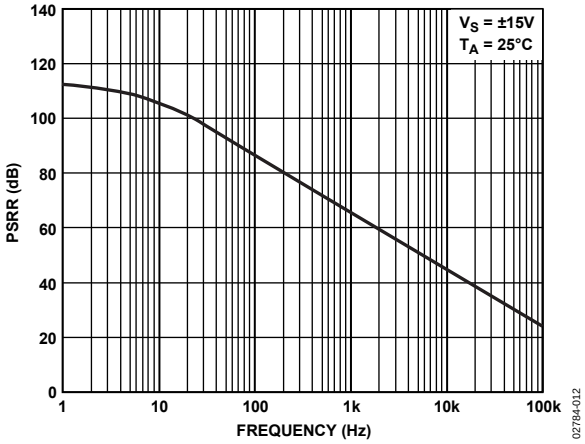

Figure 11. PSRR vs. Frequency

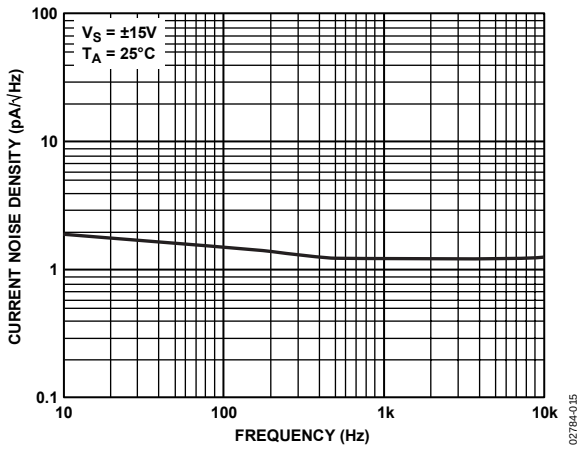

Figure 14. Current Noise Density vs. Frequency

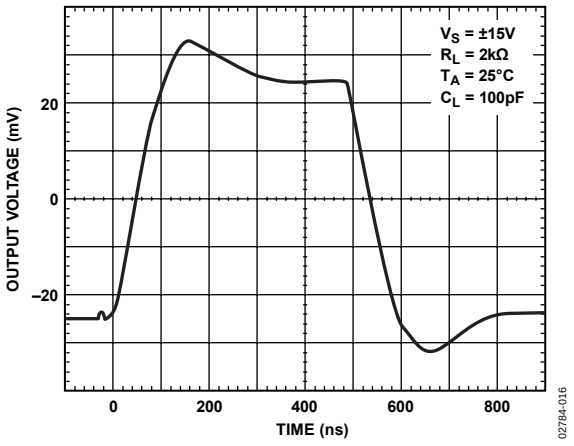

Figure 15. Transient Response

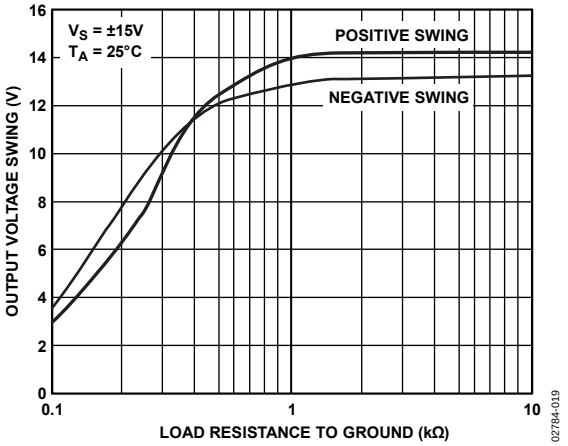

Figure 18. Output Voltage Swing vs. Load Resistance

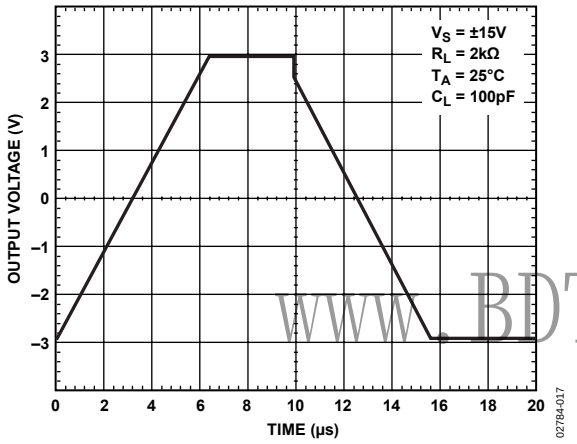

Figure 16. Voltage Follower Pulse Response

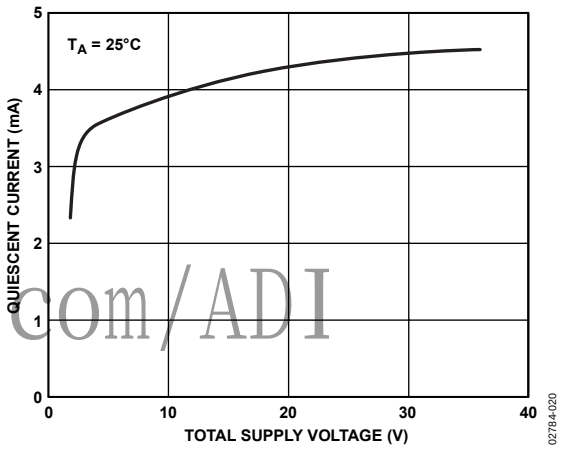

Figure 19. Quiescent Current vs. Total Supply Voltage

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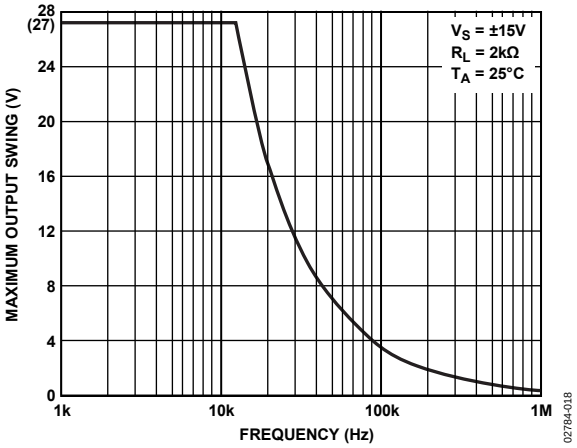

Figure 17. Maximum Output Swing vs. Frequency

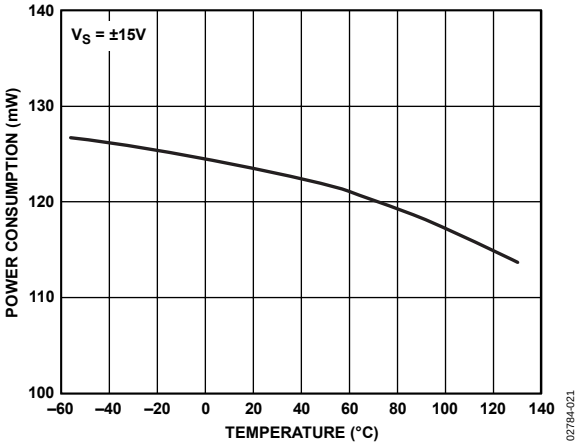

Figure 20. Power Consumption vs. Temperature

OUTLINE DIMENSIONS

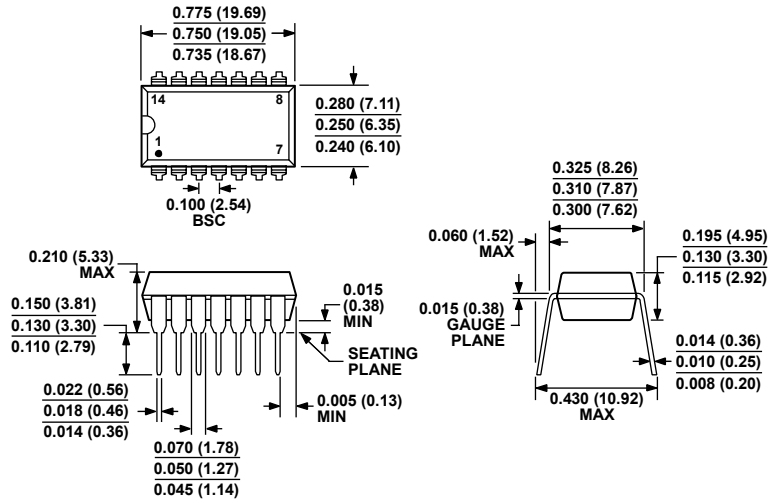

Figure 21. 14-Lead Plastic Dual In-Line Package [PDIP]
(N-14)
[P Suffix]
Dimensions shown in inches and (millimeters)

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ORDERING GUIDE

Model	Temperature Range	Package Description	Package Option
OP11EP	0°C to 70°C	14-Lead Plastic Dual In-Line Package (PDIP)	N-14 (P-Suffix)
OP11EPZ[1]	0°C to 70°C	14-Lead Plastic Dual In-Line Package (PDIP)	N-14 (P-Suffix)

[1] Z = RoHS Compliant Part.

For military processed devices, refer to the Standard Microcircuit Drawing (SMD) available at http://www.dscc.dla.mil/downloads/Milspec/Smd/89801.pdf.

SMD Part Number	Analog Devices, Inc. Equivalent
5962-89801012A	OP11ARCMDA
5962-8980101CA	OP11AYMDA

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